Amendments to the Abstract:

Please amend the abstract as printed on the front page of the PCT publication as follows.

A PLL ~~structure~~ comprises a PFD, a loop filter and a VCO, as well as a voltage shift capacitor [[(Ca)]] coupling the PFD and the VCO. A voltage shift control circuit [[(50)]] is placed in parallel with the voltage shift capacitor. This circuit comprises controlled charging means [[(51)]], which are designed to charge the voltage shift capacitor according to a channel control signal. It also comprises controlled pre-charging means [[(52)]] which are designed to accelerate the charging of the voltage shift capacitor by the controlled charging means. It further comprises controlled biasing means [[(53)]], designed to ensure the bias of the input during the pre-charging of the voltage shift capacitor.